Amendments to the Specification

Please replace the paragraph beginning on page 7, line 22 with the following amended paragraph:

The NMOS transistor 219 has the drain ~~source~~ electrode connected to the drain electrode of the PMOS transistor 211, the [[drain]] source electrode connected to the drain electrode of the NMOS transistor 215, and a gate electrode connected to the power supply potential VDD. The NMOS transistor 221 has the ~~source~~ drain electrode connected to the drain electrode of the PMOS transistor 213, the [[drain]] source electrode connected to the drain electrode of the NMOS transistor 217, and a gate electrode connected to the power supply potential VDD. The NMOS transistor 219 and the NMOS transistor 221 connected between the current mirror type load circuit and a pair of signal input transistors. These NMOS transistors 219 and 221 constitute a voltage relief element (a voltage down-converting element) which makes the voltage applied to the drain electrodes of the pair of signal input transistors ease or descent.

Please replace the paragraph beginning on page 9, line 24 with the following amended paragraph:

The signal output part 205 has a PMOS transistor 223, a [[PMOS]] NMOS transistor 225, and a NMOS transistor 227, provided between the power supply potential VPP and the ground potential VSS. The signal output part 205 outputs a signal having a second amplitude. The second amplitude is made up of the power

supply potential VPP as a logic high level and the ground potential VSS as a logic low level.

Please replace the paragraph beginning on page 10, line 3 with the following amended paragraph:

The PMOS transistor 223 has a source electrode connected to the power supply potential VPP, a drain electrode connected to an output terminal OUT, and a gate electrode connected to the drain electrode of the PMOS transistor 213. The NMOS transistor 225 has a source electrode connected to the ground potential VSS, and a drain electrode connected to the a [[drain]] source electrode of the NMOS transistor 227, and a gate electrode connected to the output terminal of the inverter 209. The PMOS transistor 223 is a transistor for charge and which supplies the power supply potential VPP to an unillustrated load connected to the output terminal OUT. The NMOS transistor 225 is a transistor for discharge and which supplies the power supply potential VSS to the unillustrated load connected to the output terminal OUT.

Please replace the paragraph beginning on page 10, line 14 with the following amended paragraph:

The NMOS transistor 227 has the ~~source~~ drain electrode connected to the output terminal OUT, the [[drain]] source electrode connected to the drain electrode of the NMOS transistor 225, and a gate electrode connected to the power supply potential

VDD. This NMOS transistor 227 constitutes the voltage relief element (voltage descent element) which makes the voltage applied to the drain electrode of the NMOS transistor 225 ease (descent).